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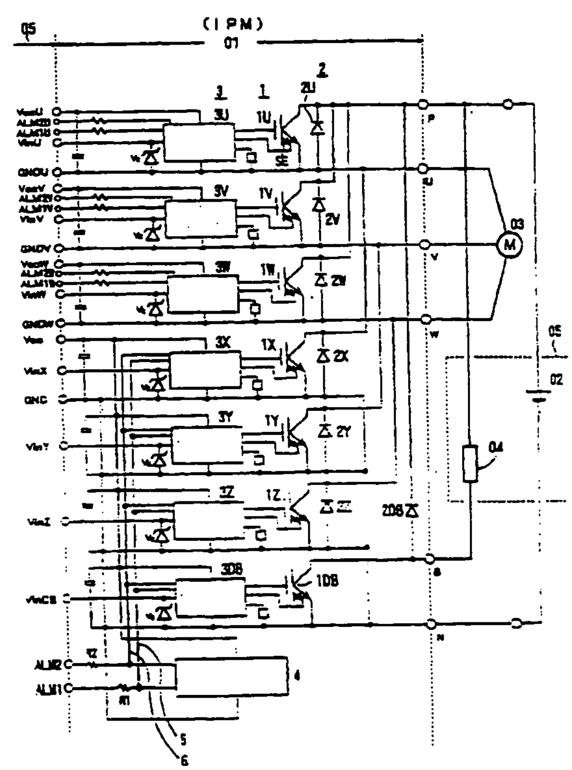
## (54) Semiconductor apparatus

(57) The object of the invention is to provide a semiconductor apparatus, including an intelligent power module, that facilitates preventing sudden stop of the inverter due to an anomaly from affecting the factory operation adversely.

Any of the protection circuits outputs an alarm signal ALM1 via an alarm enable line 5 when an anomaly is caused in the corresponding IGBT. In advance to outputting the alarm signal ALM1, when the protection circuit detects a sign of a possible anomaly from the collector current or the chip temperature of any of the IGBT's exceeding a second predetermined collector current level or the second predetermined temperature level higher than the normal collector current value or the normal chip temperature but lower than a first predetermined collector current level or a first predetermined temperature level for outputting the alarm signal ALM1, the protection circuit outputs a preliminary alarm signal ALM2 via a preliminary alarm line 6 without turning off the pertinent IGBT.

Figure 1

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## Description

[0001] The present invention relates to a semiconductor apparatus incorporated in a power converting apparatus such as an inverter for variably controlling th speed of a motor. More specifically, the present invention relates to a so-called intelligent power module (hereinafter referred to as an "IPM") that incorporates semiconductor switching devices for power conversion, driver circuits for driving the respective semiconductor switching devices and various protection circuits in a package.

[0002] Figure 6 is a block diagram showing the main portion of a conventional inverter for variably controlling the speed of a motor including an intelligent power module (IPM). In the figure, there are shown an IPM 01, a main DC power supply 02 formed of a not shown rectifier circuit in a main control board 05 of the inverter, a motor 03, the speed thereof is variably controlled by the inverter, and a resistor 04 in the main control board 05 of the inverter for consuming regenerated electric power. The resistor 04 will be described later in d tail.

[0003] The main control board 05 of the inverter includes the above described rectifier circuit that constitutes the main DC power supply 02, the control circuits which generate various control signals for controlling the IPM 01, and such control circuits.

[0004] The IPM01 includes semiconductor switching devices which also work as sensing IGBT's 1 (1U through 1Z and 1DB), each having a sensing terminal SE for dividing the emitter current thereof and for detecting anomalies in the emitter current caused by short circuit in the load and such causes. In the following, the IGBT's 1U through 1Z will be sometimes referred to as the "inverter switches" and the IGBT 1DB as the "braking switch".

[0005] The IPM01 includes free wheel diodes 2 (2U through 2Z and 2DB). Each of the free wheel diodes 2U through 2Z is connected in opposite parallel between the collector and the emitter of each of the IGBT's (inverter switches) 1U through 1Z. The free wheel diode 2DB is connected in parallel to the resistor 04 in such a polarity that the cathode of the diode 2DB is connected to the positive electrode P of the main DC power supply 02.

[0006] The IPM01 includes pre-drivers 3 (3U through 3Z and 3DB) disposed in one to one correspondence to the IGBT's 1 (1U through 1Z and 1DB). In Figure 6, one pre-driver is used to drive one IGBT. Alternatively, one pre-driver may be used to drive all the inverter switches 1U through 1Z, two pre-drivers may be used to drive the inverter switches on the upper arm and the inverter switches on the lower arm respectively, or one pre-driver may be used to drive all the inverter switches 1U through 1Z and the braking switch 1DB.

[0007] The IGBT's 1U and 1X are connected in series to each other and in forward between the positive electrode P and the negative electrode N of the main DC power supply 02 such that the IGBT 1U is on the upper arm and the IGBT 1X is on the lower arm of the inverter bridge. The IGBT's 1V and 1Y are connected in series to each other and in forward between the positive electrode P and the negative electrode N of the main DC power supply 02 such that the IGBT 1V is on the upper arm and the IGBT 1Y is on the lower arm. And, the IGBT's 1W and 1Z are connected in series to each other and in forward between the positive electrode P and the negative electrode N of the main DC power supply 02 such that the IGBT 1W is on the upper arm and the IGBT 1Z is on the lower arm.

[0008] Six inverter switches, i.e. the IGBT's 1U through 1Z, constitute a three-phase inverter bridge circuit. The mutual connection point of the IGBT's 1U and 1X is connected to an output terminal U for the U phase of a three-phase alternating current. The mutual connection point of the IGBT's 1V and 1Y is connected to an output terminal V for the V phase of the three-phase alternating current. And, the mutual connection point of the IGBT's 1W and 1Z is connected to an output terminal W for the W phase of the three-phase alternating current. The output terminals U, V and W are connected to the motor (a three-phase induction motor in Figure 6) 03. The braking switch, i.e. the IGBT 1DB, is connected in series to the resistor 04 for consuming the regenerated electric power and in forward between the P and N electrodes of the main DC power supply 02.

[0009] Each of the pre-drivers 3U through 3Z and 3DB includes a circuit for driving the gate of the corresponding IGBT and protection circuits. A driving power supply (DC 15 V in Figure 6) is fed to the pre-drivers 3U through 3Z and 3DB. Fundamentally, the pre-drivers 3U through 3Z and 3DB work as driver circuits which feed a gate signal, indicative of ON or OFF of the corresponding IGBT, between the gate and the emitter thereof, when an ON-signal or an OFF signal (hereinafter referred to as a "driver input") is inputted from the main control board 05 of the inverter to any of the terminals VinU through VinZ and VinDB, to switch on or off the corresponding IGBT.

[0010] Usually, a three-phase AC voltage, the voltage and the frequency thereof are variable, is generated through the IGBT's 1U through IZ which convert the electric power from the main DC power supply 02 to control the speed of the motor 03 variably.

[0011] When the output frequency of the inverter is decreased to decelerate or stop the motor 03 while the motor 03 is driven, the energy of the motor 03 is regenerated to the main DC power supply 02, and the voltage between the electrodes P and N of the DC power supply 02 rises. As the voltage rises to much, an over voltage exceeding the breakdown voltages of the IGBT's and the smoothing capacitor in the DC power supply 02 may be applied thereto.

[0012] To avoid this, the main control board 05 of the inverter monitors the voltage between the elec-

trodes P and N of the DC power supply 02. When the voltage between the electrodes P and N of the DC power supply 02 exceeds a predetermined value, the control circuit feeds ON and OFF signals to the input terminal VinDB of the pre-driver 3DB for the braking switch, i.e. the IGBT 1DB to intermittently switch on the IGBT 1DB. As the IGBT 1DB is switched on intermittently, the electric power regenerated from the motor 03 to the DC power supply 02 is bypassed to the resistor 04, therein the regenerated electric power is consumed. Thus, the voltage between the electrodes of the main DC power supply 02 is prevented from increasing too much.

**[0013]** The pre-drivers 3 described above exhibit the function of 1) driving of the IGBT's and various protection functions, such as 2) protection against short circuit, 3) protection against a low voltage, 4) protection against an overcurrent, and 5) protection against overheat of the IGBT's.

**[0014]** In the protection against short circuit 2), the pre-drivers 3 monitor the output currents from the sensing terminals SE of the IGBT's at a high speed. When any of the monitored output currents exceeds a predetermined level (set, for example, at a value from 4 to 5 times as large as the rated current), the pertinent pre-driver 3 turns off the corresponding IGBT in a very short time (by the so-called soft interruption that lowers the gate voltage at first and, then, turns off the IGBT) so that the pertinent IGBT may be protected.

**[0015]** The protection against a low voltage 3) is conducted to keep the gate voltages of the IGBT's at an optimum value. In the protection against a low voltage 3), the pre-drivers 3 monitor the driving voltages, which the pre-drivers 3 feed to the IGBT's. When any of the monitored driving voltages is lower than a predetermined value, the pertinent pre-driver 3 turns off the corresponding IGBT so that the IGBT may be protected.

**[0016]** In the overcurrent protection 4), the pre-drivers 3 monitors the output currents from the sensing terminals SE of the IGBT's. When any of the monitored output currents exceeds a predetermined level (set, for example, at a value from 1.5 times to twice as large as the rated current), the pertinent pre-drivers 3 turns off the corresponding IGBT. The detection speed and the detection level for the overcurrent protection 4) are different from those for the short circuit protection 2).

**[0017]** In the overheat protection 5), the pre-drivers 3 monitor the temperatures of the chips, in which the respective IGBT's are buried, by detecting the forward currents of the diodes buried in the chips. When any of the monitored temperatures exceeds a predetermined temperature, the pertinent pre-driver 3 turns off the corresponding IGBT.

**[0018]** There is shown an overheat protection circuit 4 in the bottom of Figure 6. Usually, the signal on an alarm enable line 5 is set at a high level Hi. When any of the temperatures of metallic or ceramic insulation substrates, which insulate the chips of the IGBT's 1U through 1Z and 1DB from the respective metallic radiator substrates, exceeds a predetermined temperature, the overheat protection circuit 4 sets the signal on the alarm enable line 5, usually at a high level Hi, at a low level Lo to output an alarm signal ALM at the low level Lo.

**[0019]** When any of the pre-drivers 3X through 3Z, which drive the IGBT's 1X through 1Z constituting the lower arm of the inverter bridge circuit, executes any of the protection operations 2) through 4) the pertinent pre-driver 3X, 3Y or 3Z sets the signal on the alarm enable line 5 at the low level Lo to output an alarm signal ALM at the low level Lo, similarly as the overheat protection circuit 4 does.

**[0020]** When the alarm signal ALM is outputted, i.e. when alarm enable line 5 is active, the pre-drivers which have not outputted the alarm signal ALM detect the alarm signal ALM at the low level Lo and turn off the respective IGBT's.

**[0021]** When the main control board 05 of the inverter detects the alarm signal ALM at the low level Lo, the main control board 05 of the inverter outputs an OFF-signal to the pre-drivers 3U through 3W which drive the IGBT's 1U through 1W on the upper arm of the inverter bridge circuit to turn off the IGBT's 1U through 1W.

**[0022]** Thus, when any of the pre-drivers 3U through 3Z and 3DB and the overheat protection circuit 4 executes any of the protection operations, all the IGBT's 1U through 1Z and 1DB are turned off.

**[0023]** As described above, the conventional IPM exhibits the protection functions mainly to protect the semiconductor devices which the IPM incorporates against anomalies and to avoid breakdown of the semiconductor devices. As soon as the IPM detects an anomaly, all the IGBT's are turned off to stop the operations of the inverter.

**[0024]** Therefore, if an anomaly is caused in the inverter, breakdown of the semiconductor devices will be avoided. However, when an inverter, operated in a manufacturing line in an unnoticeable overloaded state, suddenly stops, the operation of an entire factory system slows down or stops.

**[0025]** Especially in a large manufacturing line, tremendous loses are caused. Therefore, it is desired to avoid slowdown or stop of the operation of the factory system by detecting a sign indicating possible anomalous stop of the inverter, by outputting a preliminary alarm signal and by guiding the operators of the inverter to remove the causes which may cause anomalous stop of the inverter in advance to real anomalous stop of the inverter.

**[0026]** As described above, as soon as any of the pre-drivers 3X through 3Z for the inverter switches detects an anomaly, the signal on the alarm enable lin 5 is set at the low level Lo, thereby the operation of the braking switch, i.e. IGBT 1DB, is also stopped.

**[0027]** When the operation of the inverter circuit is

stopped suddenly by an anomaly caused in the inverter switches, the energy of the rotating motor 03, i.e. a load, is regenerated back to the main DC power supply 02, and the voltage across the main DC power supply 02 is raised.

[0028] As described above, when the main control board 05 of the inverter detects the rise of the voltage across the main DC power supply 02, the control circuit makes the braking IGBT 1DB work to suppress the rise of the voltage across the main DC power supply 02 in usual. However, once the pre-driver 3DB, that detected the low signal level Lo on the alarm enable line 5, has turned off the braking IGBT 1DB, the braking IGBT 1DB never operates even when an ON-signal is fed to the input terminal VinBD of the pre-driver 3DB. Therefore, the voltage across the main DC power supply 02 is not prevented from rising, and, in the worst case, breakdown of the constituent elements of the IPM is caused.

[0029] In view of the foregoing, it is an object of the invention to provide a semiconductor apparatus including an IMP that facilitates outputting a preliminary alarm signal without stopping the inverter when a sign of an anomaly in the IPM is detected, guiding removal of the causes which may cause anomalous stop of the inv rter, and preventing the operation of the factory system from sudden slowdown or sudden stop. It is another object of the invention to provide a semiconductor apparatus including an IMP that facilitates intermittently switching on the braking IGBT and, thereby, preventing the voltage across the main DC power supply from rising even when any of the inverter switches is turned off due to an anomaly and the inverter is stopped.

[0030] According to a first aspect of the invention, there is provided a semiconductor apparatus including one or more semiconductor switching devices for electric power conversion, one or more driver circuits disposed in one to one correspondence to the one or more semiconductor switching devices, the one or more driver circuits switching on and off corresponding one of the one or more semiconductor switching devices via the respective control terminals in response to an ON/OFF command inputted thereto from the outside, and one or more anomaly protection means disposed in one to one correspondence to the one or more semiconductor switching devices, the one or more anomaly protection means monitoring corresponding one of the one or more semiconductor switching devices, the one or more anomaly protection means ordering corresponding one of the one or more driver circuits to turn off the corresponding one of the one or more semiconductor switching devices when the one or more anomaly protection means have detected an anomaly in the corresponding one of the one or more semiconductor switching devices, the semiconductor apparatus further including: one or more anomaly predicting means disposed in one to one correspondence to the one or more semiconductor switching devices, the one or more anomaly predicting means outputting a preliminary alarm signal when the one or more anomaly predicting means have detected a sign of an anomaly in corr - sponding one of the one or more semiconductor switching devices.

[0031] Advantageously, the one or more anomaly protection means judge that an anomaly is caused in corresponding one of the one or more semiconductor switching devices when the current flowing between the main terminals of the corresponding one of the one or more semiconductor switching devices has exceeded a first predetermined value higher than the normal value of the current, and the one or more anomaly predicting mean output the preliminary alarm signal when the current flowing between the main terminals of the corresponding one of the one or more semiconductor switching devices has exceeded a second predetermined value higher than the normal value of the current but lower than the first predetermined value.

[0032] Advantageously, the one or more anomaly protection means judge that an anomaly is caused in corresponding one of the one or more semiconductor switching devices when the chip temperature of the corresponding one of the one or more semiconductor switching devices has exceeded a first predetermined temperature higher than the normal chip temperature, and the one or more anomaly predicting mean output the preliminary alarm signal when the chip temperature of the corresponding one of the one or more semiconductor switching devices has exceeded a second predetermined temperature higher than the normal chip temperature but lower than the first predetermined temperature.

[0033] Advantageously, the one or more anomaly protection means output an alarm signal when the one or more anomaly protection means judge that the anomaly is caused in the corresponding one of the one or more semiconductor switching devices.

[0034] Advantageously, the preliminary alarm signal and the alarm signal are digital signals, the pulse widths thereof are different from each other, and the digital signals are outputted from a common output terminal.

[0035] According to a second aspect of the invention, there is provided a semiconductor apparatus including: an inverter for driving a motor, the inverter including a main circuit; the main circuit including one or more inverter semiconductor switches; a braking semiconductor switch, the braking semiconductor switch interrupting and making flow a current, thereby to consume energy regenerated from the motor; driver circuits disposed in one to one correspondence to the one or more inverter semiconductor switches and the braking semiconductor switch, the driver circuits switching on and off the corresponding one of the one or more inverter semiconductor switch s and the braking semiconductor switch via the respective control terminals in response to an ON/OFF command inputted thereto from the outside; anomaly protection means disposed in

one to one correspondence to the one or more inverter semiconductor switches and the braking semiconductor switch, the anomaly protection means monitoring corresponding one of the one or more inverter semiconductor switching devices and the braking semiconductor switching device, the anomaly protection m ans ordering corresponding one of the driver circuits to turn off the corresponding one of the one or more inverter semiconductor switches and the braking semiconductor switch when the anomaly protection means have detected an anomaly in the corresponding one of the one or more inverter semiconductor switches and the braking semiconductor switch; alarm signal outputting means disposed in one to one correspondence to the one or more inverter semiconductor switches and the braking semiconductor switch, each of the alarm signal outputting means outputting an alarm signal through a common signal line when an anomaly is caused in corresponding one of the one or more inverter semiconductor switches and the braking semiconductor switch; and one or more alarm signal receiving means disposed in one to one correspondence to the one or more inverter semiconductor switches, the one or more alarm signal receiving means order corresponding one of the anomaly protection means to turn off corresponding one of the one or more inverter semiconductor switches in response to the alarm signal inputted from the alarm signal outputting means of the other inverter semiconductor switch through the common signal line.

**[0036]** Advantageously, the one or more alarm signal receiving means turn off the one or more inverter semiconductor switches.

**[0037]** The characteristic functions of the semiconductor apparatus according to the invention are as follows.

**[0038]** According to the first aspect of the invention, as soon as a sign of an anomaly in any of the inverter switches is detected, the IPM outputs a preliminary alarm signal ALM2, without stopping the electric power conversion, in advance to turning off the inverter switches to remove the cause of the anomaly.

**[0039]** The sign of an anomaly in any of the inverter switches is detected at an instance when the collector current or the chip temperature of any of the inverter switches exceeds a predetermined value higher than the normal value but lower than the anomalous value.

**[0040]** When a common terminal is used for outputting the alarm signal indicating an anomaly from the IPM and for outputting the preliminary alarm signal indicating a sign of an anomaly from the IPM, the pulse widths of the alarm signal and the preliminary alarm signal are set to be different from each other.

**[0041]** The preliminary detection of a sign of an anomaly facilitates removing the causes which may cause a real anomaly and avoiding anomalous sudden stop of the inverter in advance.

**[0042]** According to the second aspect of the invention, when an anomaly is caused in any of the inverter switches and the braking switch, the corresponding predriver turns off the pertinent switch and outputs an alarm signal via a common signal line. The other predrives of the inverter switches, which have received the alarm signal via the common signal line, turn off the corresponding inverter switches.

**[0043]** The pre-driver for the braking switch does not turn off the braking switch even when an alarm signal is outputted from any of the pre-drivers for the inverter switches.

**[0044]** Even when the inverter stops suddenly and the power supply voltage rises due to the regenerated energy from the motor, the power supply voltage is prevented from further rising by consuming the regenerated energy by the ON/OFF operation of the braking switch.

**[0045]** Now the invention will be explained hereinafter with reference to the accompanying drawings which illustrate the preferred embodiment of the invention. Throughout the following drawing figures, the same reference numerals as used in Figure 6 are used to designate the same or corresponding constituent elements.

Figure 1 is a block diagram showing the main portion of an inverter for variably controlling the speed of a motor according to the first embodiment of the invention including an intelligent power module (IPM) 01;

Figure 2 shows timing charts for explaining the overheat protection according to the second embodiment of the invention;

Figure 3 shows timing charts for explaining the overcurrent protection according to the first embodiment of the invention;

Figure 4 shows the wave forms of the alarm signal and the preliminary alarm signal on the common alarm signal line according to the third embodiment of the invention;

Figure 5 shows timing charts for explaining the operations of the braking IGBT according to the fourth embodiment of the invention; and

Figure 6 is a block diagram showing the main portion of a conventional inverter for variably controlling the speed of a motor including an intelligent power module (IPM).

**[0046]** Referring now to Figure 1, the IPM 01 includes pre-drivers 3X through 3Z and 3DB which output an alarm signal ALM 1 to a main control board 05 of the inverter via an alarm enable line 5. The inverter according to the first embodiment is different from the conventional inverter in that the inverter according to the first embodiment includes a preliminary alarm line 6, through which the pre-drivers 3X through 3Z and 3DB output a preliminary alarm signal ALM 2, and in that the pre-drivers 3U through 3W for the inverter switches on the upper arm also output respective alarm signals ALM1U through ALM1W and respective preliminary

alarm signals ALM2U through ALM2W.

[0047] By making the pre-drivers 3U through 3W output respective alarm signals ALM1U through ALM1W and respective preliminary alarm signals ALM2U through ALM2W, more precise control may be executed. The functions of the pre-drivers same with the conventional pre-divers may be assigned to one or less number of pre-drivers.

[0048] Figure 3 shows timing charts for explaining the overcurrent protection according to the first embodiment. The timing chart (a) in Figure 3 shows a typical wave form of an ON/OFF command (driver input) VinX, VinY, VinZ or VinDB inputted to the pre-driver 3X, 3Y, 3Z or 3DB from the main control board 05 of the inverter. The timing chart (b) in Figure 3 shows a typical wave form of a collector current of any of the IGBT's 1X through 1Z and 1DB flowing in response to the foregoing ON/OFF command when an overcurrent anomaly is caused.

[0049] The timing chart (c) in Figure 3 shows the output timing of the preliminary alarm signal ALM2 outputted from the pertinent pre-driver 3X, 3Y, 3Z or 3DB based on the collector current (b) of Figure 3. The timing chart (d) in Figure 3 shows the output timing of the alarm signal ALM1.

[0050] Even when the upper arm of the inverter is not provided with the alarm output function, the wave forms (a) and (b) in Figure 3 are applied also to the inverter switches 1U through 1W on the upper arm. The pre-drivers 3U through 3W for the inverter switches on the upper arm also execute protecting operation at an alarm level Im1 of the collector current, although the pr -drivers 3U through 3W do not output the alarm signal ALM 1.

[0051] As shown in Figure 3, when the pre-driver, 3X, 3Y, 3Z or 3DB detects anomalous increase of the collector current of the corresponding IGBT that reaches the alarm level Im1 at a time t1, thé pertinent pre-driver, 3X, 3Y, 3Z or 3DB stops the operation of the corresponding IGBT, in the same manner as the conventional inverter does, and sets the signal on the alarm enable line 5 at a low level Lo to output an alarm signal ALM1. In advance, as soon as the collector current exceeding the normal value reaches a preliminary alarm level Im2 at a time t2, the pertinent pre-driver, 3X, 3Y, 3Z or 3DB sets the signal on the preliminary alarm line 6 at a low level Lo to output a preliminary alarm signal ALM2 to the main control board 05 of the inverter.

[0052] As far as only the preliminary alarm signal ALM2 is outputted, the corresponding IGBT is not turned off. The low signal level Lo on the preliminary alarm line 6 does not affect the other pre-drivers connected to the preliminary alarm line 6.

[0053] Figure 2 shows timing charts for explaining the overheat protection acc rding to the second embodiment of the invention. The timing chart (a) in Figure 2 shows a typical wave form of a driver input VinX, VinY, VinZ or VinDB inputted to the pre-driver 3X, 3Y, 3Z or 3DB from the main control board 05 of the inverter. The timing chart (c) in Figure 2 shows a typical wave form of a collector current of any of the IGBT's 1X through 1Z and 1DB flowing in response to the foregoing driver input. The timing chart (b) in Figure 2 shows a typical temperature change, including anomalous heat up of the IGBT chip, caused by the collector current of (c) in Figure 2.

[0054] The timing chart (d) in Figure 2 shows the output timing of the preliminary alarm signal ALM2 outputted from the pertinent pre-driver 3X, 3Y, 3Z or 3DB based on the chip temperature detection in (b) of Figure 2. The timing chart (e) in Figure 2 shows the output timing of the alarm signal ALM1.

[0055] The wave forms (a) and (c) in Figure 2 are applied also to the inverter switches 1U through 1W on the upper arm. The pre-drivers 3U through 3W for the inverter switches on the upper arm also execute protecting operation at an alarm level θ m1 for the temperature of the corresponding IGBT chip, although the pre-drivers 3U through 3W do not output the alarm signal ALM 1.

[0056] As shown in Figure 2, when the pre-driver, 3X, 3Y, 3Z or 3DB detects anomalous heat up of the corresponding IGBT chip that reaches the alarm level θ m1 (from 160 to 170°) at a time t1, the pertinent pre-driver, 3X, 3Y, 3Z or 3DB stops the operation of the corresponding IGBT, in the same manner as the conventional inverter does, and sets the signal on the alarm enable line 5 at a low level Lo to output an alarm signal ALM1. In advance, as soon as the chip temperature exceeding the normal value reaches the preliminary alarm level θ m2 (e.g. 130°) at a time t2, the pertinent pre-driver, 3X, 3Y, 3Z or 3DB sets the signal on the preliminary alarm line 6 at a low level Lo to output a preliminary alarm signal ALM2 to the main control board 05 of the inverter.

[0057] As far as only the preliminary alarm signal ALM2 is outputted, the corresponding IGBT will not be turned off. The low signal level Lo on the preliminary alarm line 6 does not affect the other pre-drivers connected to the preliminary alarm line 6.

[0058] In the first and second embodiments, the alarm enable line 5 for outputting the alarm signal ALM1 and the preliminary alarm line 6 for outputting the preliminary alarm signal ALM2 are used. Alternatively, one alarm signal line may be used commonly for outputting the alarm signal ALM1 and for outputting the preliminary alarm signal ALM2. (That is, the conventional output terminals used for outputting the alarm signal ALM1 may be used also for outputting the preliminary alarm signal ALM2.)

[0059] Figure 4 shows the wave forms of the alarm signals and the preliminary alarm signal on a common alarm signal line (i.e. on the common output terminal for utputting the alarm signals). As shown in Figure 4, the output width T2, for which the signal is set at the low level Lo, for the preliminary alarm signal ALM2 and the

output width T1, for which the signal is set at the low level Lo, for the alarm signal ALM1 are different so that these alarm signals ALM1 and ALM2 are distinguishable form each other.

[0060] In Figure 3 or 2, when the collector current or the chip temperature, that has been increasing after the preliminary alarm signal ALM2 was outputted, reaches the alarm level Im1 or θ m1 for outputting the alarm signal ALM1, the pertinent pre-driver 3X, 3Y, 3Z or 3DB turns off the corresponding IGBT, sets the signal on the alarm enable line 5 at the low level Lo and outputs the alarm signal ALM1 at the low signal level Lo to the main control board 05 of the inverter.

[0061] As soon as the other pre-drivers, which did not output the alarm signal ALM1, detect the low signal level Lo on the alarm enable line 5, the other pro-drivers turn off the corresponding IGBT's.

[0062] In contrast, according to the fourth embodiment of the invention, the pro-driver 3DB for the breaking switch does not turn off the corresponding IGBT 1DB even when the signal on the alarm enable line 5 is set at the low level Lo.

[0063] According to the fourth embodiment of the invention, even when the signal on the alarm enable line 5 is set at the low level Lo in association with the protecting operation and the output of the alarm signal ALM1 by any of the pro-drivers 3X through 3Z connected to the alarm enable line 5, the pro-driver 3DB for the braking IGBT 1DB does not turn off the IGBT 1DB so that the IGBT 1DB may keep executing the switching operation (as far as the pro-driver 3DB has not outputted the alarm signal ALM1).

[0064] Figure 5 shows timing charts for explaining the operation of the braking IGBT 1DB according to the fourth embodiment of the invention.

[0065] The timing chart (a) in Figure 5 shows a typical wave form of an ON/OFF command (driver input) VinX, VinY or VinZ inputted to the pro-driver 3X, 3Y or 3Z from the main control board 05 of the inverter. The timing chart (b) in Figure 5 shows a typical wave form of a collector current of any of the IGBT's 1X through 1Z flowing in response to the foregoing ON/OFF command when an overcurrent anomaly is caused.

[0066] The timing chart (c) in Figure 5 shows the output timing of the alarm signal ALM1 outputted from the pertinent pre-driver 3X, 3Y or 3Z based on the collector overcurrent (b) of Figure 5. The timing chart (d) in Figure 5 shows the change of the voltage between the electrodes P and N of the main DC power supply 02 with elapse of time.

[0067] The timing chart (e) in Figure 5 shows the output timing of the ON/OFF command (driver input) VinDB from the main control board 05 of the inverter, that monitors the voltage (d) in Figure 5 across the main DC power supply 02, to the pre-driver 3DB for the braking IGBT 1DB. The timing chart (f) in Figure 5 shows the timing, thereat a current flows through the braking IGBT 1DB switched on and off based on the driver input VinDB of (e) in Figure 5.

[0068] Note that (e) and (f) in Figure 5 show macroscopic transitions with elapse of time. In practice, the ON signal at the low level Lo of the driver input VinDB is an ON/OFF signal with a short period. The current (f) in Figure 5 through the braking switch 1DB has a wave form corresponding to the driver input VinDB shown by (e) in Figure 5.

[0069] As soon as the pre-driver, 3X, 3Y or 3Z detects anomalous increase of the collector current of the corresponding IGBT that reaches the alarm level Im1 at a time t1, the pertinent pre-driver, 3X, 3Y or 3Z stops the operation of the corresponding IGBT, in the same manner as the conventional inverter does, and sets the signal on the alarm enable line 5 at a low level Lo to output an alarm signal ALM1. At the same time, the other pre-drivers, which have detected the low signal level Lo on the alarm enable line 5, turn off the corresponding IGBT's on the lower arm.

[0070] All the IGBT's on the upper arm of the inverter are also turned off in response to the OFF command outputted from the main control board 05 of the inverter that has detected the alarm signal ALM1. As all the IGBT's on the upper and lower arms are turned off, the voltage between the P and N electrodes of the main DC power supply 02 is raised by the energy regenerated from the motor 03.

[0071] As soon as the main control board 05 of the inverter detects that the voltage between the P and N electrodes of the main DC power supply 02 exceeding a predetermined value at a time t3, the main control board 05 of the inverter outputs the driver input VinDB, that is an ON command (strictly describing an ON/OFF signal with a short period) to the pre-driver 3DB for the braking IGBT 1DB to intermittently switch on the braking IGBT 1DB. By intermittently switching on the braking IGBT 1DB, the energy regenerated from the motor is consumed by the resistor 04 so that the voltage across the main DC power supply 02 may be prevented from rising and an over voltage exceeding the breakdown voltages of the semiconductor devices and such constituent elements of the IMP may not be applied thereto.

[0072] According to the first aspect of the invention, the intelligent power module (IPM), that is a semiconductor apparatus incorporating semiconductor switching devices, pre-drivers and control circuits in a package, outputs a preliminary alarm signal ALM2, without stopping the power conversion, as soon as a sign of an anomaly in any of the inverter switches is detected, in advance to turning off the inverter switches to remove the anomaly caused in any of the inverter switches. The sign of an anomaly in any of the inverter switches is detected at a time when the collector current or the chip temperature of any of the inverter switches exceeds a predetermined value higher than the normal value but lower than the anomalous value. The IMP according to the first aspect of the invention facilitates removing the causes which may cause a real anomaly

in advance and avoiding anomalous sudden stop of the inverter that may affect the factory operation very badly.

**[0073]** In the IMP according to the second aspect of the invention that incorporates semiconductor switching devices constituting the bridge circuit for power conversion (inverter switches), a semiconductor switching device for interrupting and making flow a current for consuming the regenerated energy from a motor (braking switch), pre-drivers and control circuits thereof in a package, any of the protection circuits turns off corresponding one of the inverter switches and the braking switch and outputs an alarm signal via a common signal line when an anomaly is caused in the corresponding one of the inverter switches and the braking switch. The other pre-drives of the inverter switches, which have received the alarm signal via the common signal line, turn off the corresponding inverter switches, but the pre-driver for the braking switch does not turn off the braking switch even when an alarm signal is outputted from any of the pre-drivers for the inverter switches.

**[0074]** Therefore, even when the inverter stops suddenly and the power supply voltage rises due to the regenerated energy from the motor, the power supply voltage is prevented from further rising by consuming the regenerated energy by intermittently switching on the braking switch. Thus, the over voltage exceeding the breakdown voltages of the semiconductor devices and such constituent elements of the IMP may not be applied thereto.

## Claims

1. A semiconductor apparatus including

   one or more semiconductor switching devices for electric power conversion,
   one or more driver circuits disposed in one to one correspondence to said one or more semiconductor switching devices, said one or more driver circuits switching on and off corresponding one of said one or more semiconductor switching devices via the respective control terminals in response to an ON/OFF command inputted thereto from the outside, and
   one or more anomaly protection means disposed in one to one correspondence to said one or more semiconductor switching devices, said one or more anomaly protection means monitoring corresponding one of said one or more semiconductor switching devices, said one or more anomaly protection means ordering corresponding one of said one or more driver circuits to turn off said corresponding one of said one or more semiconductor switching devices when said one or more anomaly protection means have detected an anomaly in said corresponding one of said one or more semiconductor switching devices,

   said semiconductor apparatus comprising:

   one or more anomaly predicting means disposed in one to one correspondence to said one or more semiconductor switching devices, said one or more anomaly predicting means outputting a preliminary alarm signal when said one or more anomaly predicting means have detected a sign of an anomaly in corresponding one of said one or more semiconductor switching devices.

2. The semiconductor apparatus according to Claim 1, wherein said one or more anomaly protection means judge that an anomaly is caused in corresponding one of said one or more semiconductor switching devices when the current flowing between the main terminals of said corresponding one of said one or more semiconductor switching devices has exceeded a first predetermined value higher than the normal value of said current, and said one or more anomaly predicting mean output said preliminary alarm signal when said current flowing between said main terminals of said corresponding one of said one or more semiconductor switching devices has exceeded a second predetermined value higher than said normal value of said current but lower than said first predetermined value.

3. The semiconductor apparatus according to Claim 1 or 2, wherein said one or more anomaly protection means judge that an anomaly is caused in corresponding one of said one or more semiconductor switching devices when the chip temperature of said corresponding one of said one or more semiconductor switching devices has exceeded a first predetermined temperature higher than the normal chip temperature, and said one or more anomaly predicting mean output said preliminary alarm signal when said chip temperature of said corresponding one of said one or more semiconductor switching devices has exceeded a second predetermined temperature higher than said normal chip temperature but lower than said first predetermined temperature.

4. The semiconductor apparatus according to any of Claims 1 through 3, wherein said one or more anomaly protection means output an alarm signal when said one or more anomaly protection means judge that said anomaly is caused in said corresponding one of said one or more semiconductor switching devices.

5. The semiconductor apparatus according to Claim 4, wherein said preliminary alarm signal and said alarm signal are digital signals, the pulse widths thereof are different from each other, and said dig-

ital signals are outputted from a common output terminal.

6. A semiconductor apparatus comprising:

an inverter for driving a motor, said inverter including a main circuit;
said main circuit comprising one or more inverter semiconductor switches;
a braking semiconductor switch, said braking semiconductor switch interrupting and making flow a current, thereby to consume energy regenerated from said motor;
driver circuits disposed in one to one correspondence to said one or more inverter semiconductor switches and said braking semiconductor switch, said driver circuits switching on and off said corresponding one of said one or more inverter semiconductor switches and said braking semiconductor switch via the respective control terminals in response to an ON/OFF command inputted thereto from the outside;
anomaly protection means disposed in one to one correspondence to said one or more inverter semiconductor switches and said braking semiconductor switch, said anomaly protection means monitoring corresponding one of said one or more inverter semiconductor switches and said braking semiconductor switch, said anomaly protection means ordering corresponding one of said driver circuits to turn off said corresponding one of said one or more inverter semiconductor switches and said braking semiconductor switch when said anomaly protection means have detected an anomaly in said corresponding one of said one or more inverter semiconductor switches and said braking semiconductor switch;
alarm signal outputting means disposed in one to one correspondence to said one or more inverter semiconductor switches and said braking semiconductor switch, each of said alarm signal outputting means outputting an alarm signal through a common signal line when an anomaly is caused in corresponding one of said one or more inverter semiconductor switches and said braking semiconductor switch; and
one or more alarm signal receiving means disposed in one to one correspondence to said one or more inverter semiconductor switches, said one or more alarm signal receiving means order corresponding one of said anomaly protection means to turn off corresponding one of said one or more inverter semiconductor switches in response to said alarm signal inputted from said alarm signal outputting means of the other inverter semiconductor switch through said common signal line.

7. The semiconductor apparatus according to Claim 6, wherein said one or more alarm signal receiving means turn off said one or more inverter semiconductor switches.

**Figure 1**

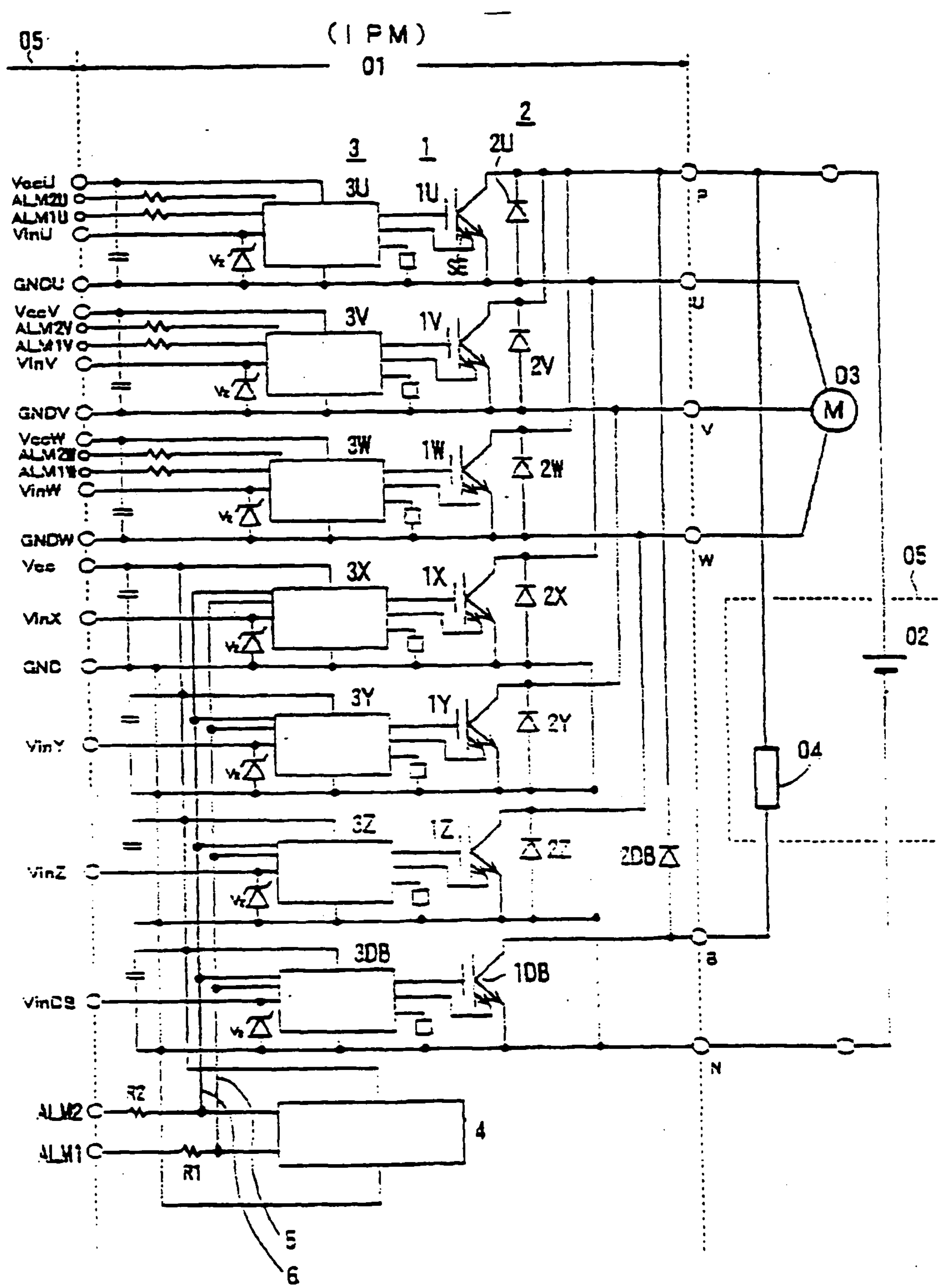

(IPM)
01
05
2
3
1
2U
3U
1U
VccU
ALM2U
ALM1U
VinU
GNDU
VccV
ALM2V
ALM1V
VinV
3V
1V
2V
GNDV
VccW
ALM2W
ALM1W
VinW
3W
1W
2W
GNDW
Vcc
3X
1X
2X
VinX
GND
3Y
1Y
2Y
VinY
3Z
1Z
2Z
VinZ
2DB
3DB
1DB
VinDB
ALM2
ALM1
R2
R1
4
5
6
P
U
V
W
B
N
03
M
05
02
04

Figure 2

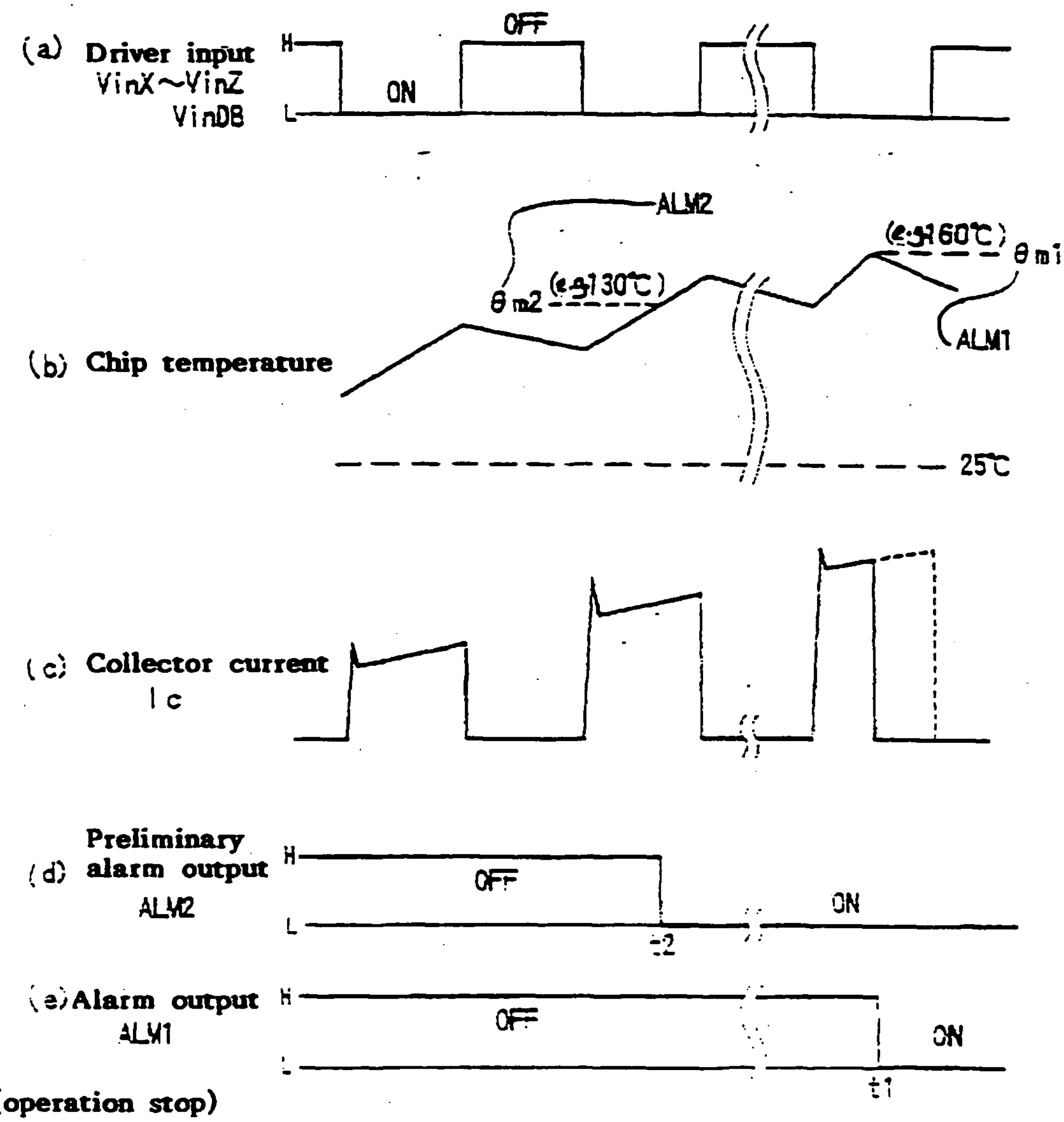

(a) Driver input
VinX~VinZ
VinDB
H
L
OFF
ON
ALM2
(e.g.160℃)
θm1
θm2
(e.g.130℃)
ALM1
(b) Chip temperature
25℃
(c) Collector current
Ic
(d) Preliminary alarm output
ALM2
H
L
OFF
ON
t2
(e) Alarm output
ALM1
H
L
OFF
ON
t1
(operation stop)

Figure 3

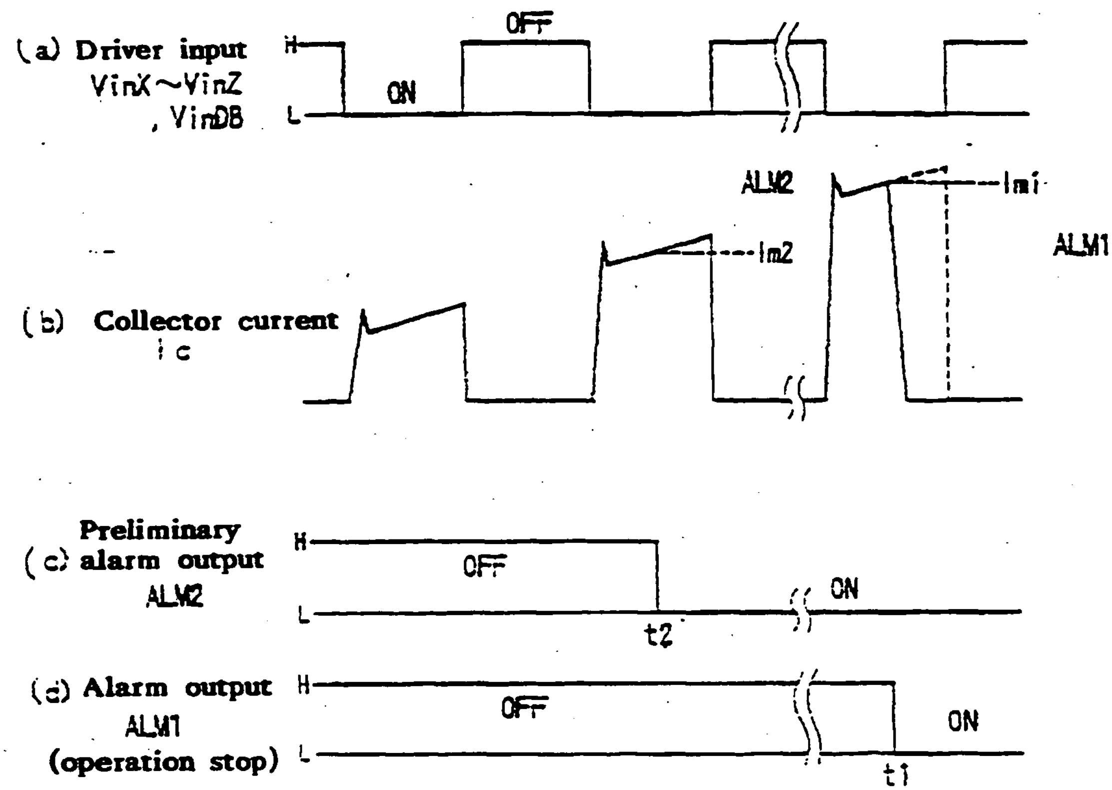



Figure 4

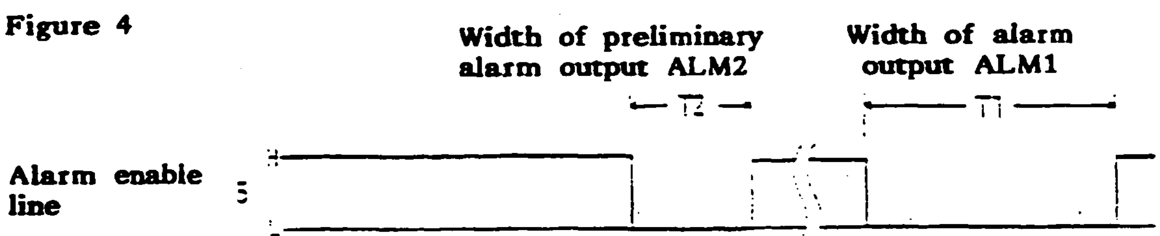


Figure 5

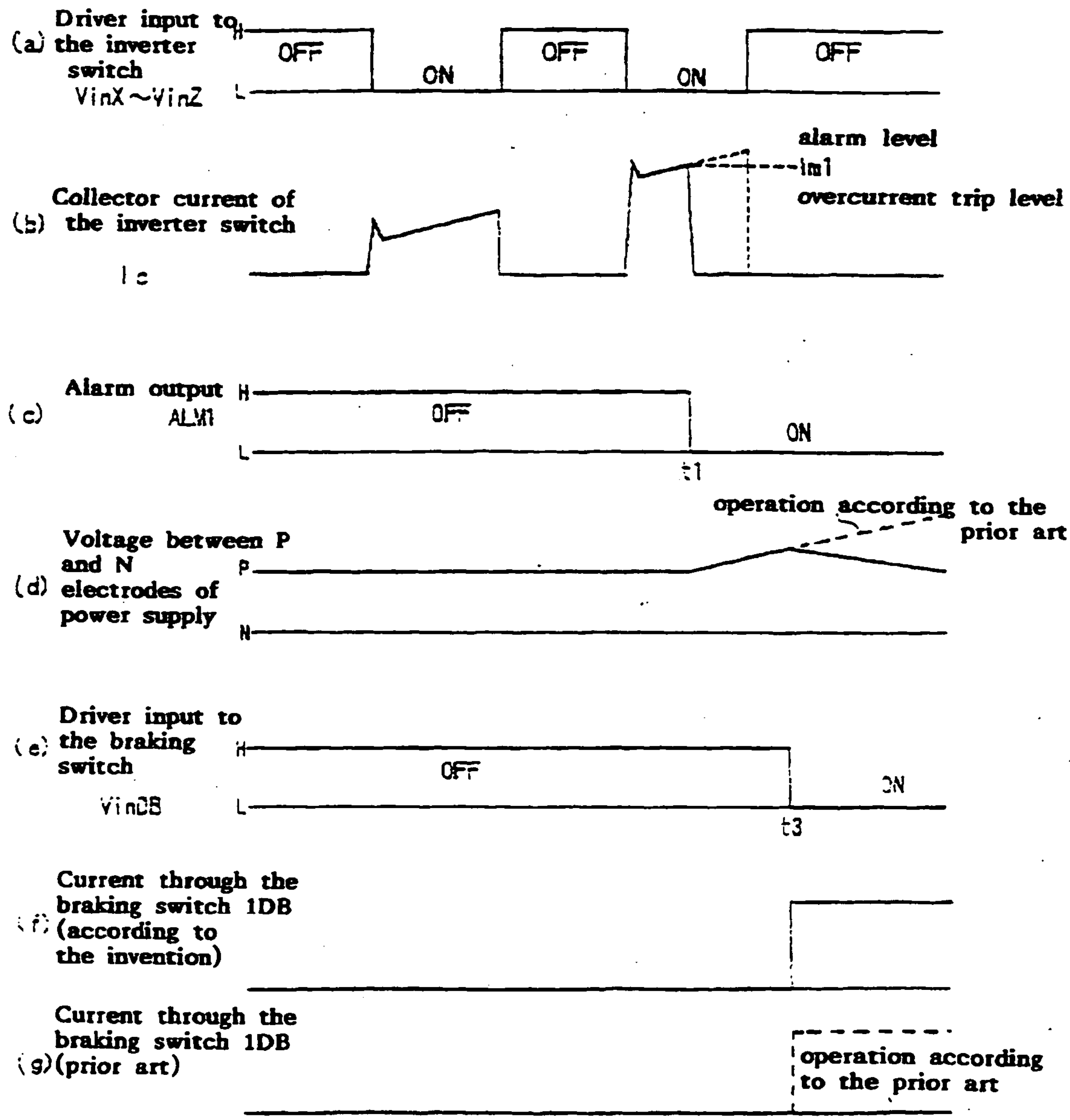
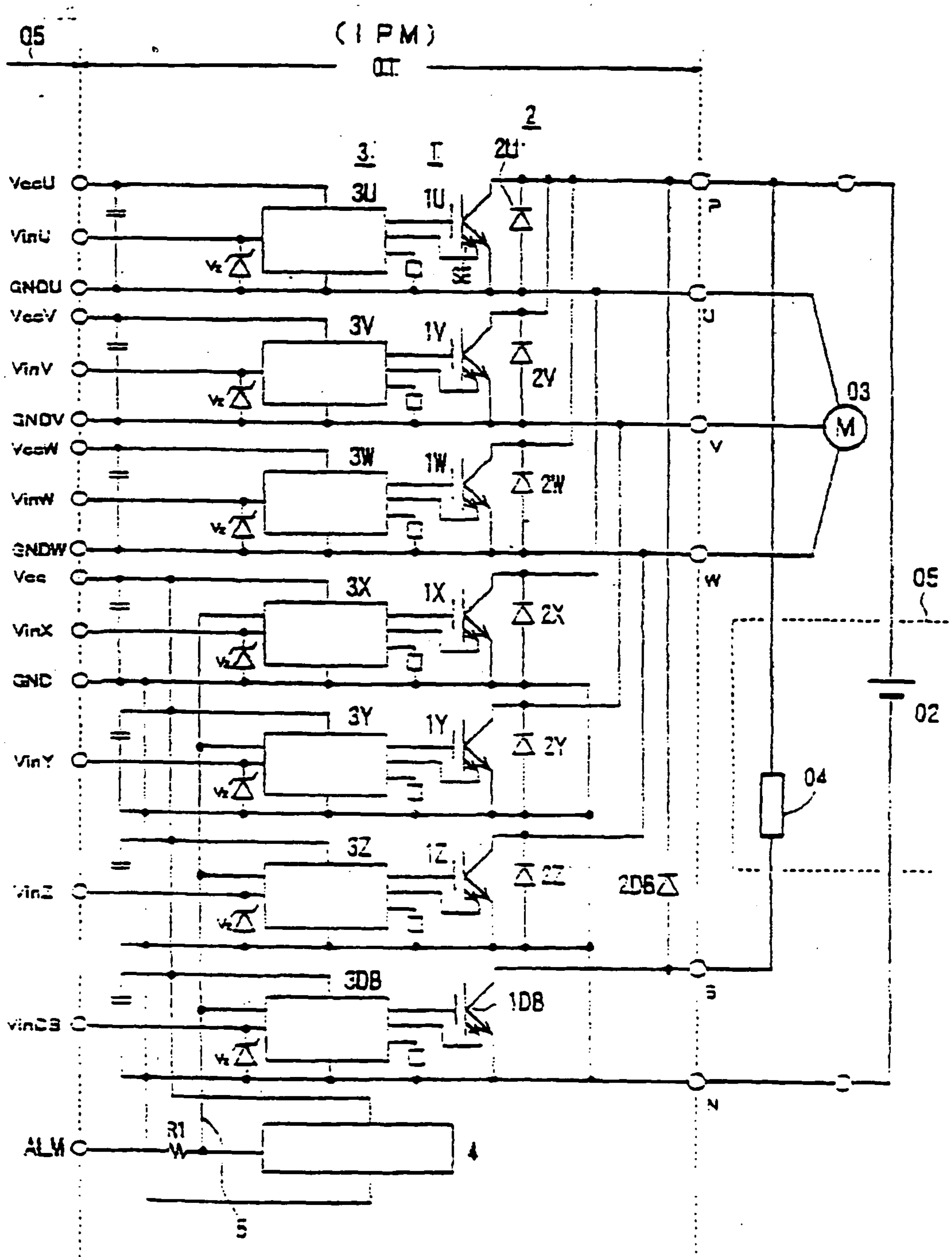

(a) Driver input to the inverter switch
VinX~VinZ
H
L
OFF
ON
OFF
ON
OFF
(b) Collector current of the inverter switch
Ic
alarm level
Im1
overcurrent trip level
(c) Alarm output
ALM1
H
L
OFF
ON
t1
(d) Voltage between P and N electrodes of power supply
P
N
operation according to the prior art
(e) Driver input to the braking switch
VinDB
H
L
OFF
ON
t3
(f) Current through the braking switch 1DB (according to the invention)
(g) Current through the braking switch 1DB (prior art)
operation according to the prior art

**Figure 6**


05
(IPM)
3
1
2
2U
VccU
VinU
GNDU
VccV
VinV
GNDV
VccW
VinW
GNDW
Vcc
VinX
GND
VinY
VinZ
VinDB
ALM
3U
3V
3W
3X
3Y
3Z
3DB
1U
1V
1W
1X
1Y
1Z
1DB
2V
2W
2X
2Y
2Z
2DB
P
U
V
W
N
03
M
05
02
04
R1
4
5